FIG.1

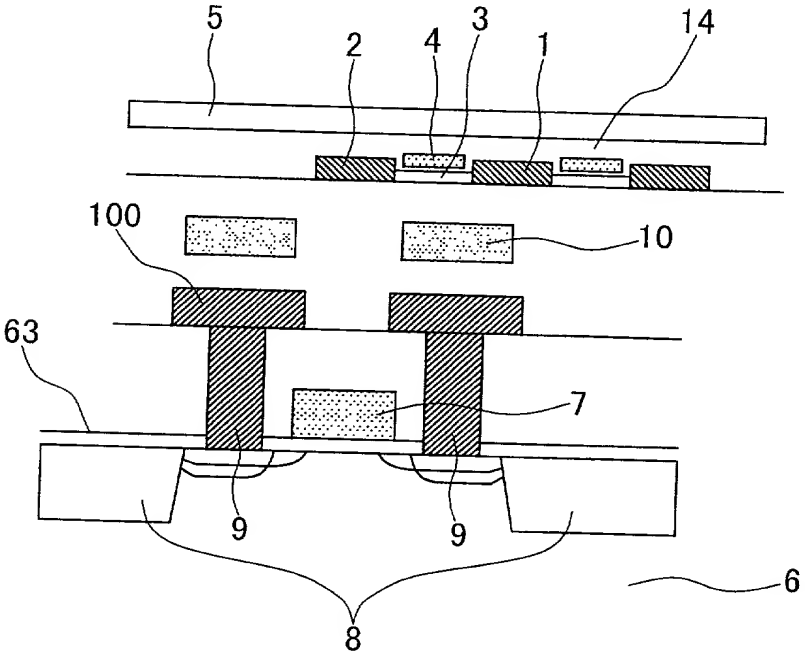


FIG.2a

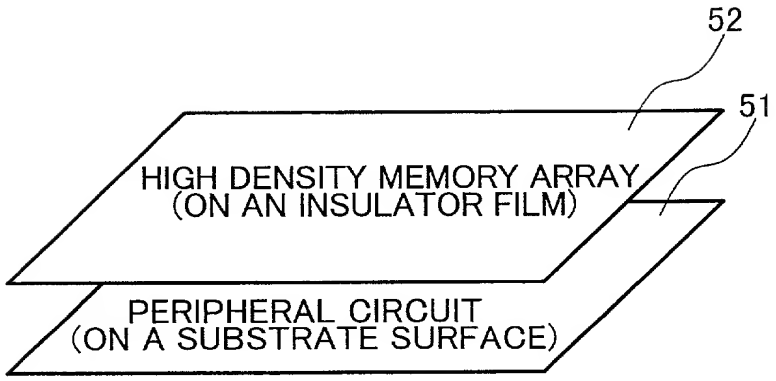

52
51
HIGH DENSITY MEMORY ARRAY
(ON AN INSULATOR FILM)
PERIPHERAL CIRCUIT
(ON A SUBSTRATE SURFACE)

FIG.2b

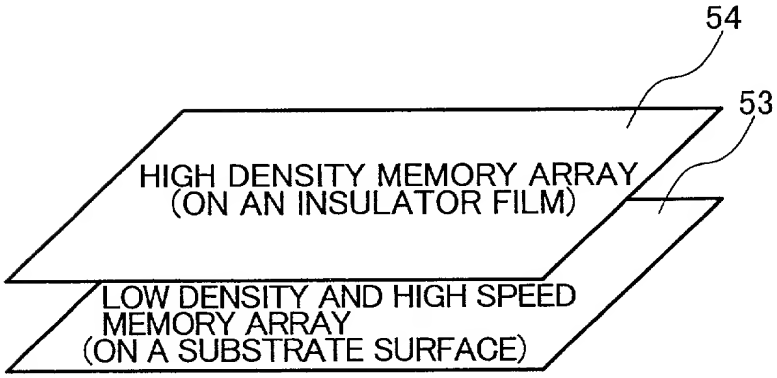

54
53
HIGH DENSITY MEMORY ARRAY
(ON AN INSULATOR FILM)
LOW DENSITY AND HIGH SPEED
MEMORY ARRAY
(ON A SUBSTRATE SURFACE)

FIG.3

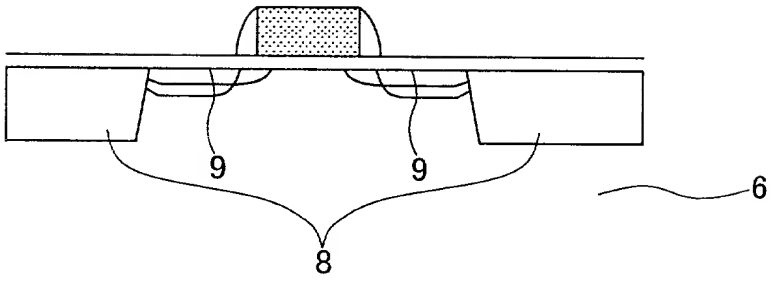


FIG.4

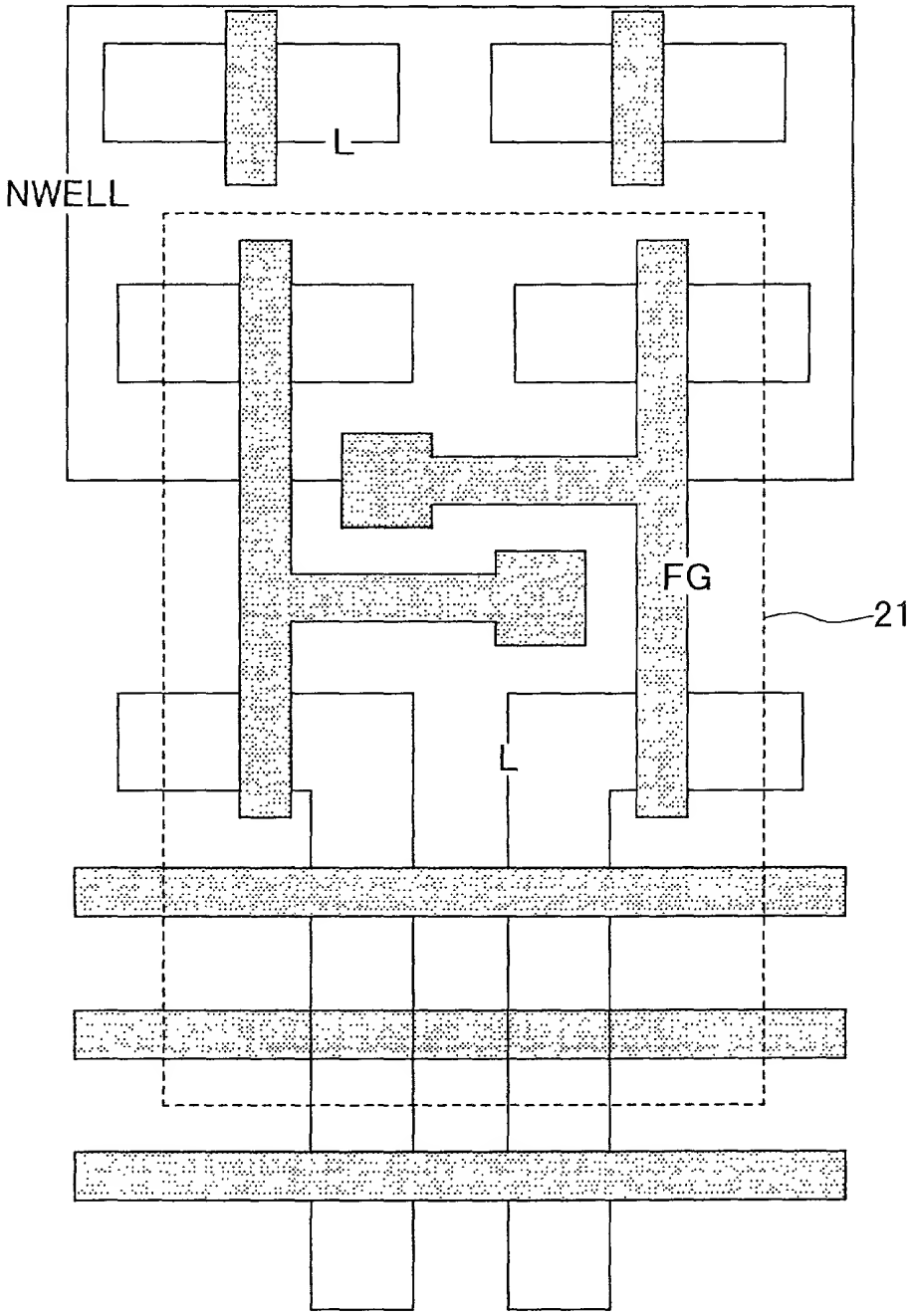


FIG.5

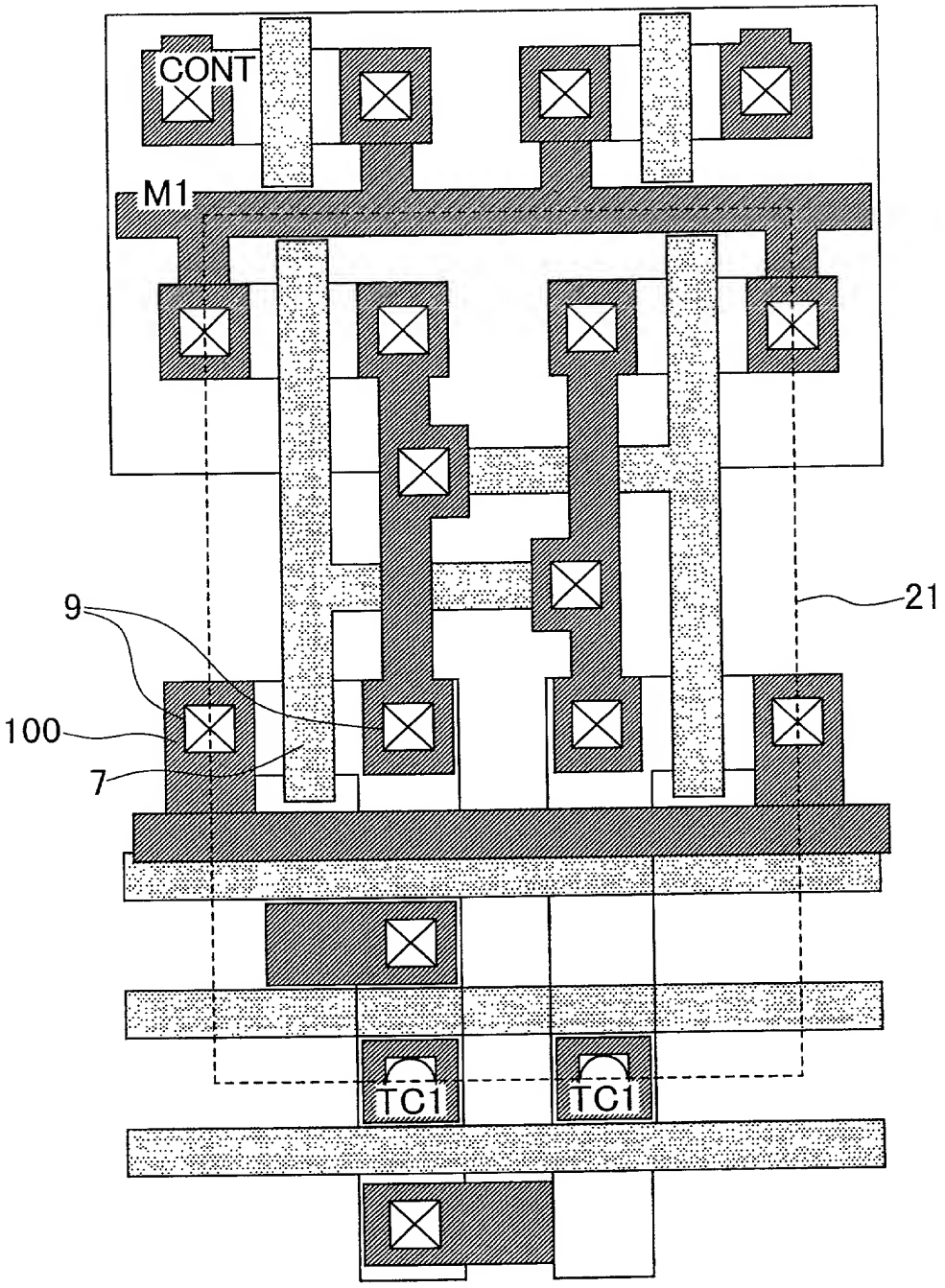


FIG.6

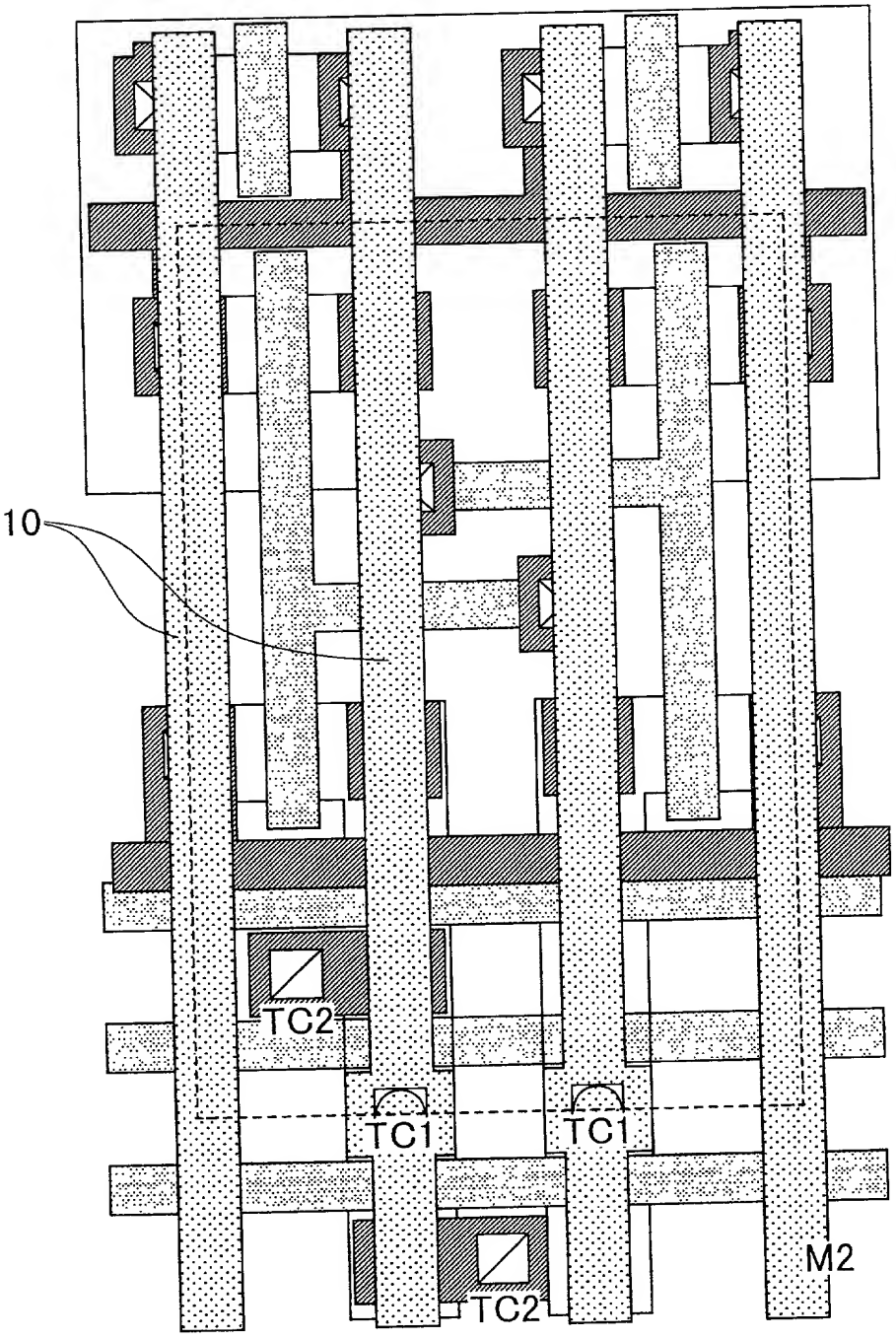


FIG.7

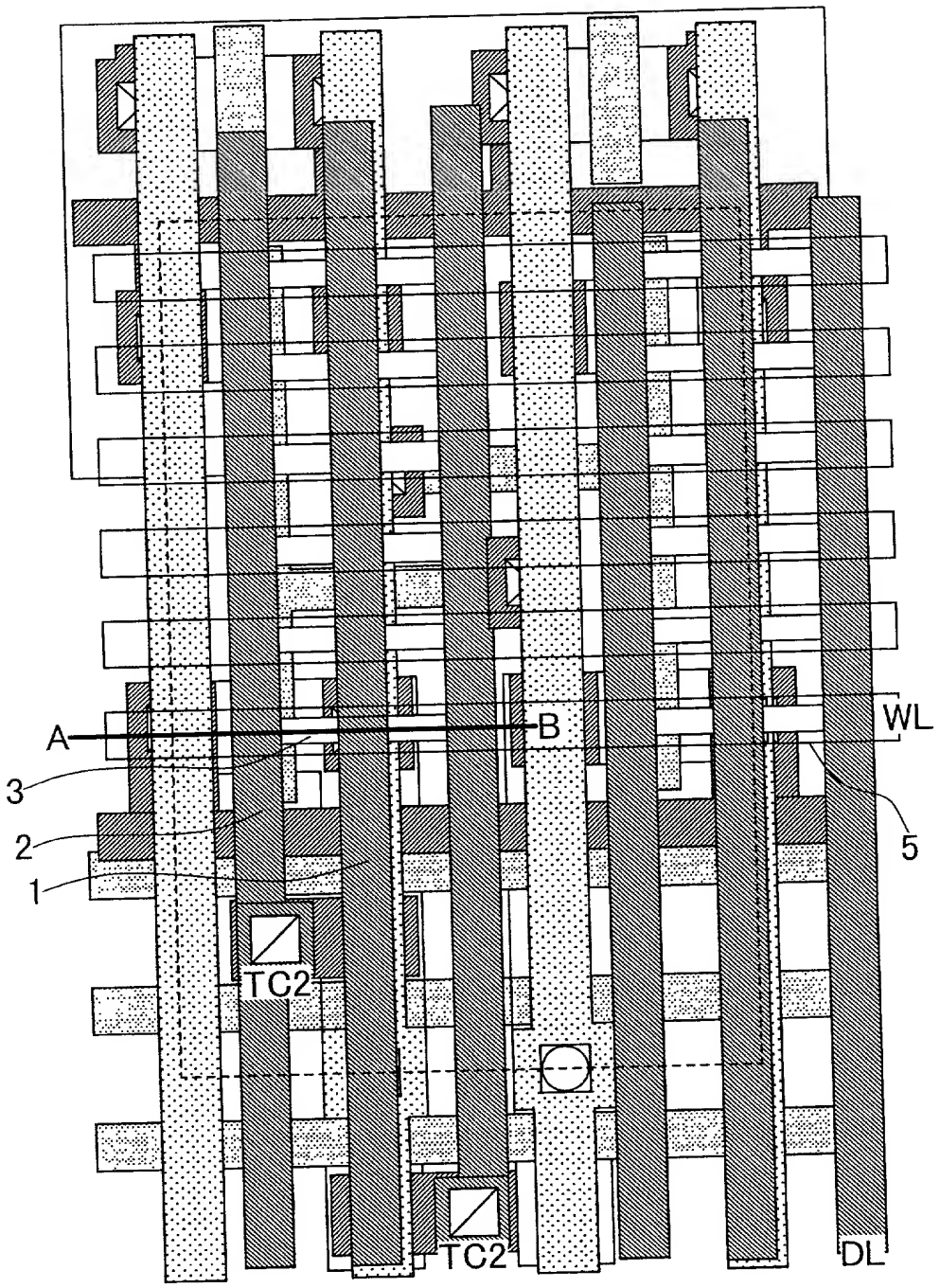


FIG.8

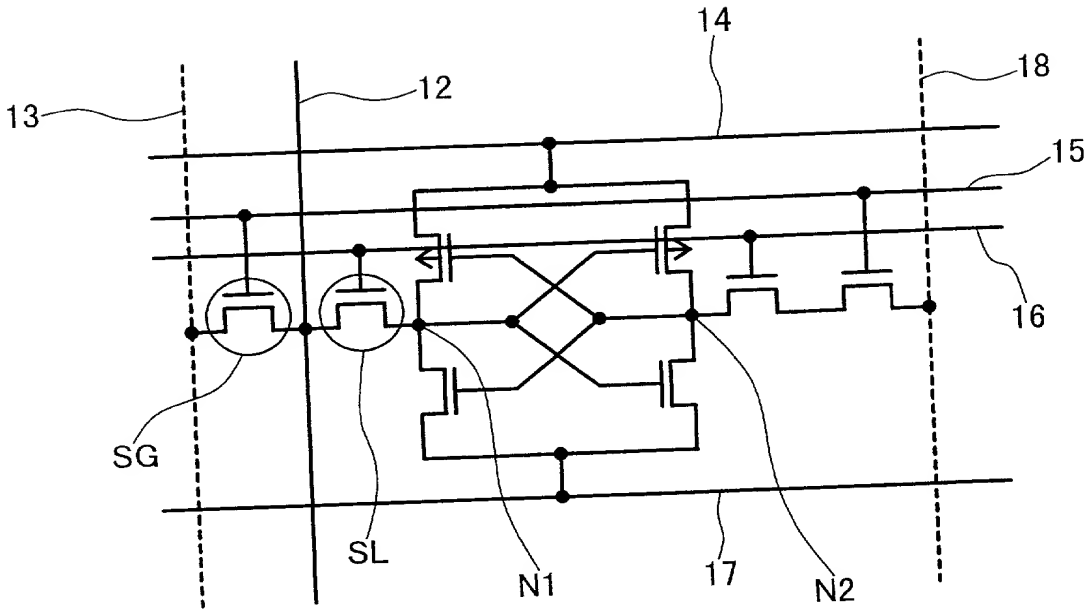


FIG.9

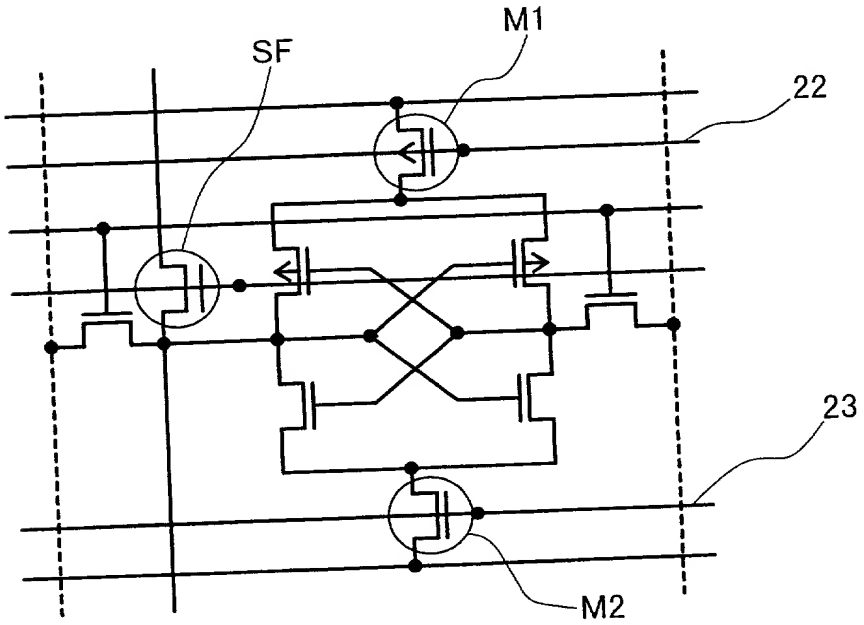


FIG.10

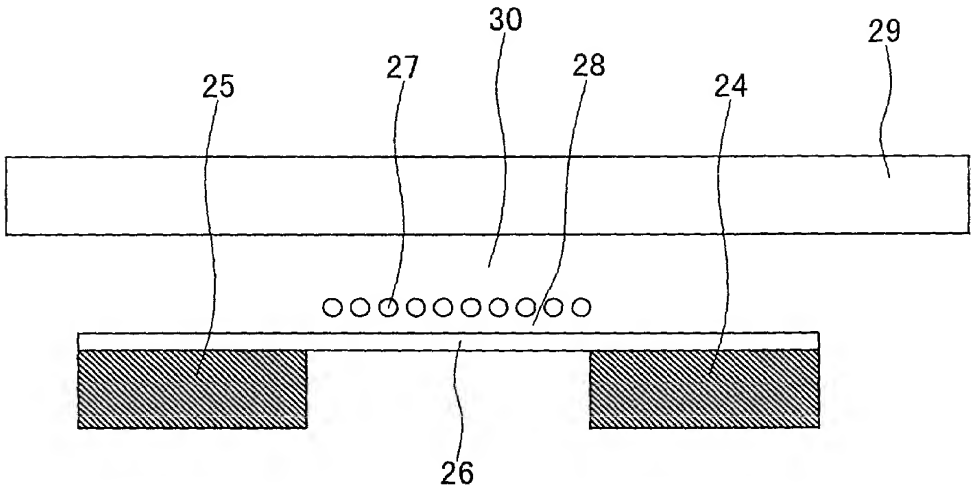


FIG.11

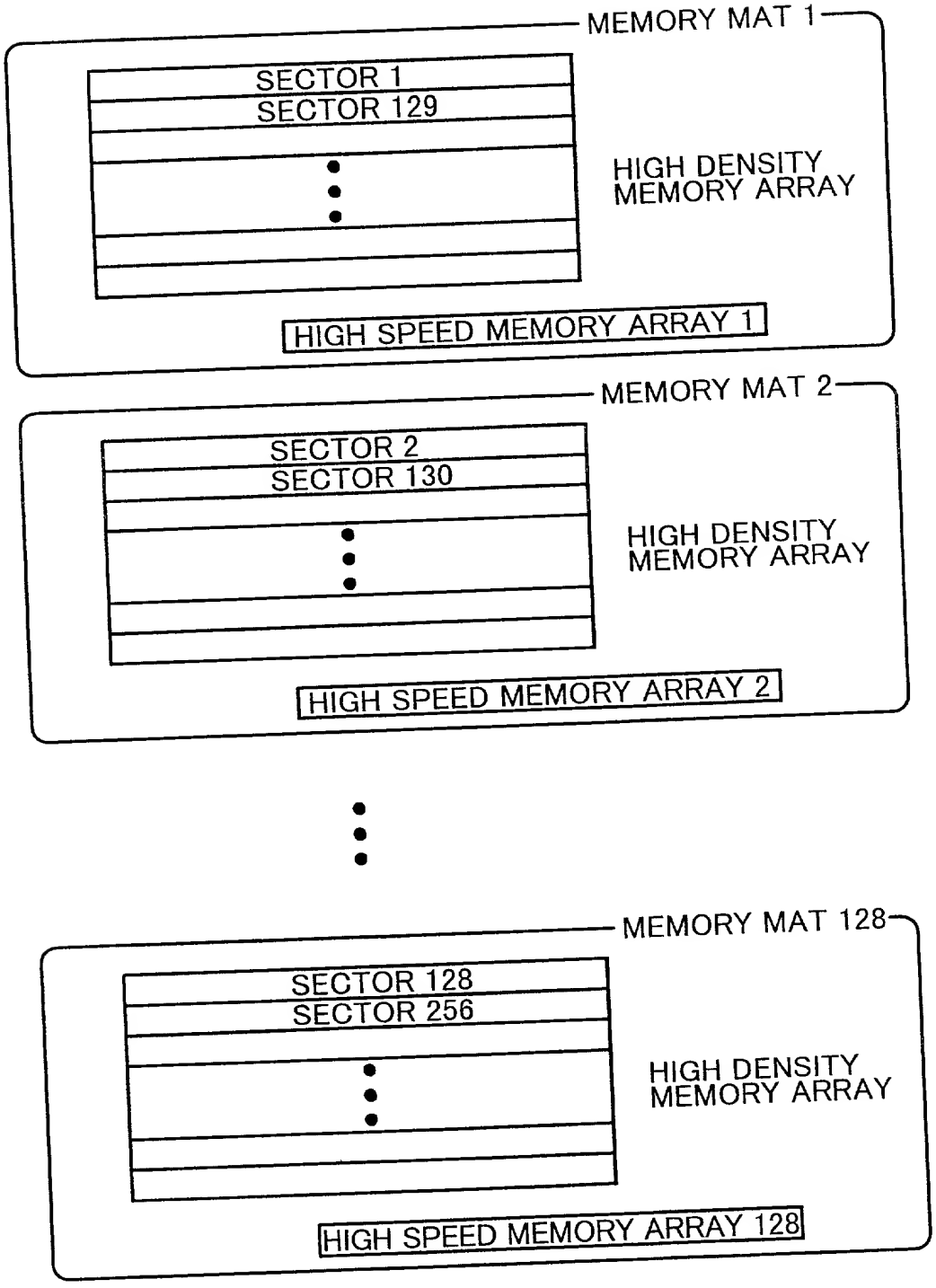

MEMORY MAT 1
SECTOR 1
SECTOR 129
HIGH DENSITY MEMORY ARRAY
HIGH SPEED MEMORY ARRAY 1
MEMORY MAT 2
SECTOR 2
SECTOR 130
HIGH DENSITY MEMORY ARRAY
HIGH SPEED MEMORY ARRAY 2
MEMORY MAT 128
SECTOR 128
SECTOR 256
HIGH DENSITY MEMORY ARRAY
HIGH SPEED MEMORY ARRAY 128

FIG.12

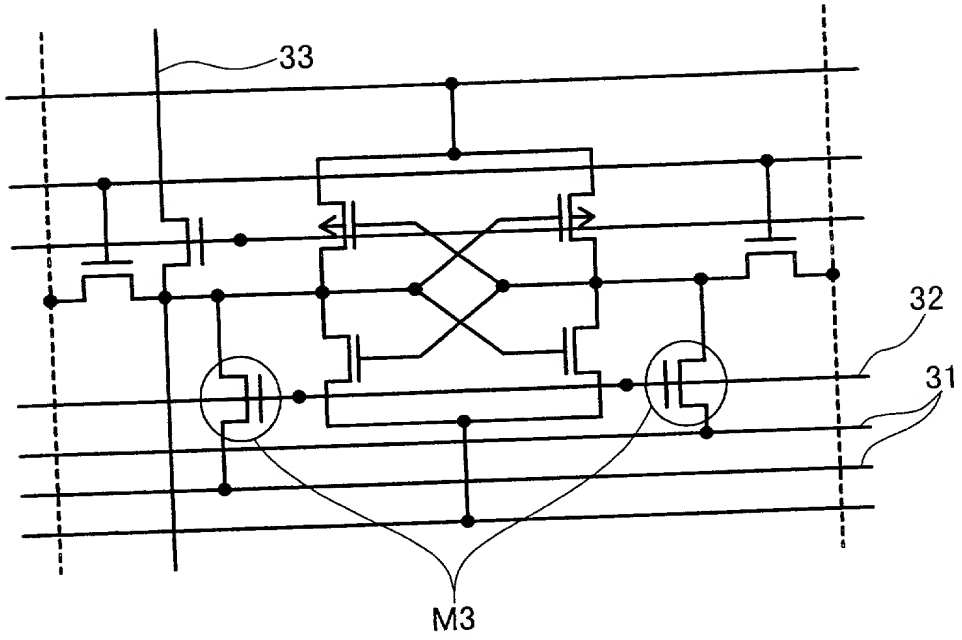


FIG.13

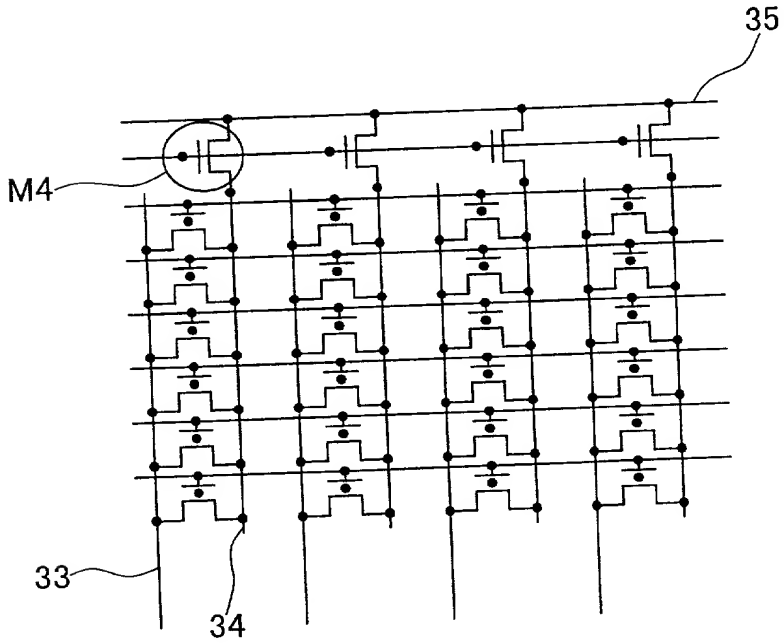


FIG.14

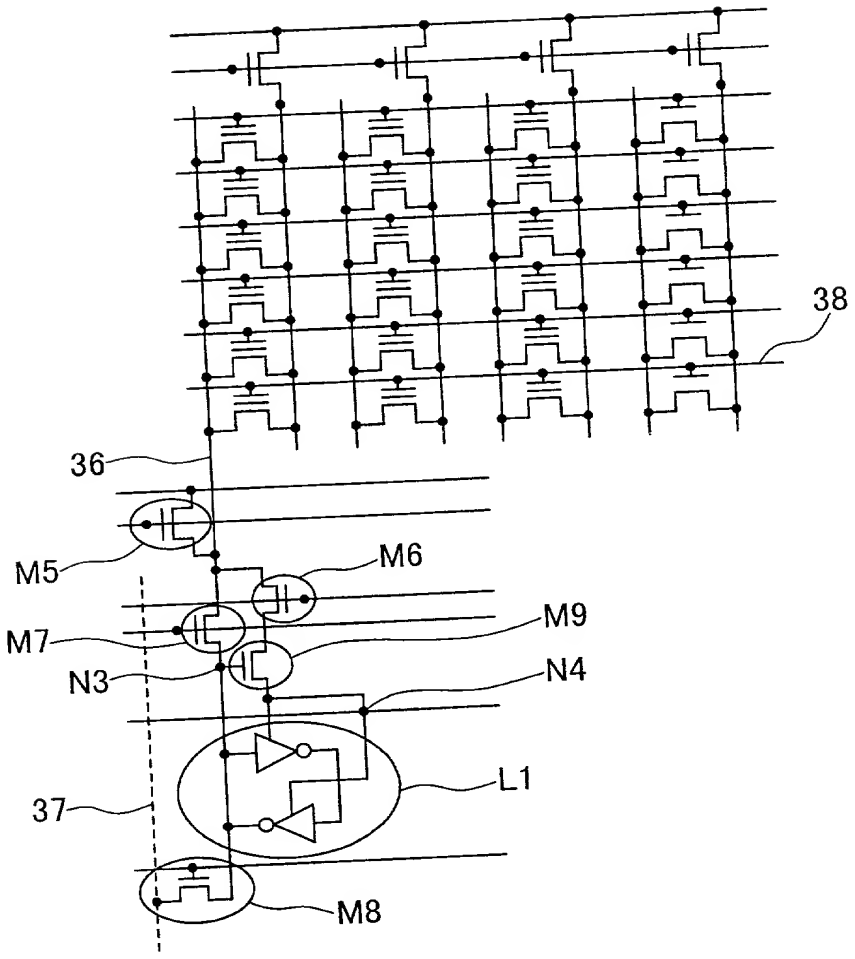


FIG.15a

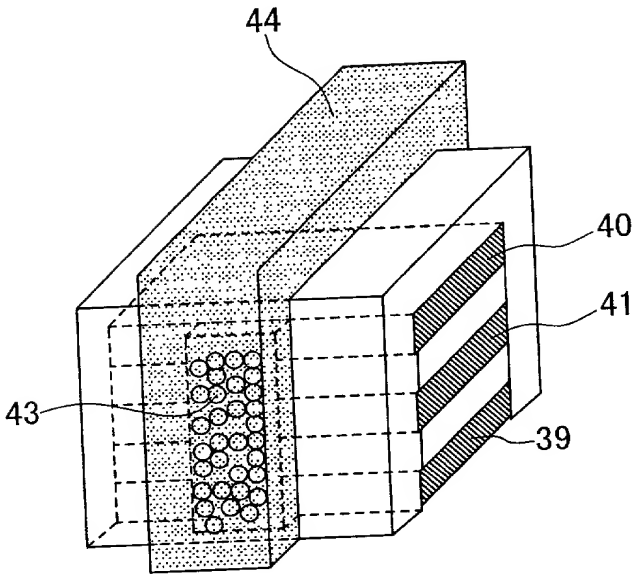


FIG.15b

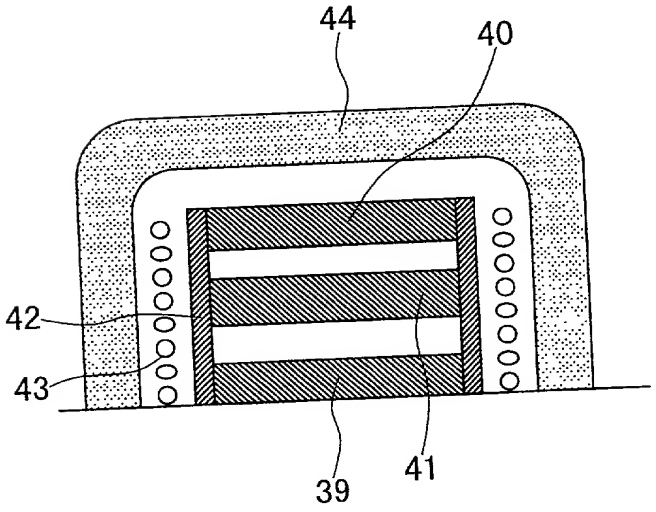


FIG.16

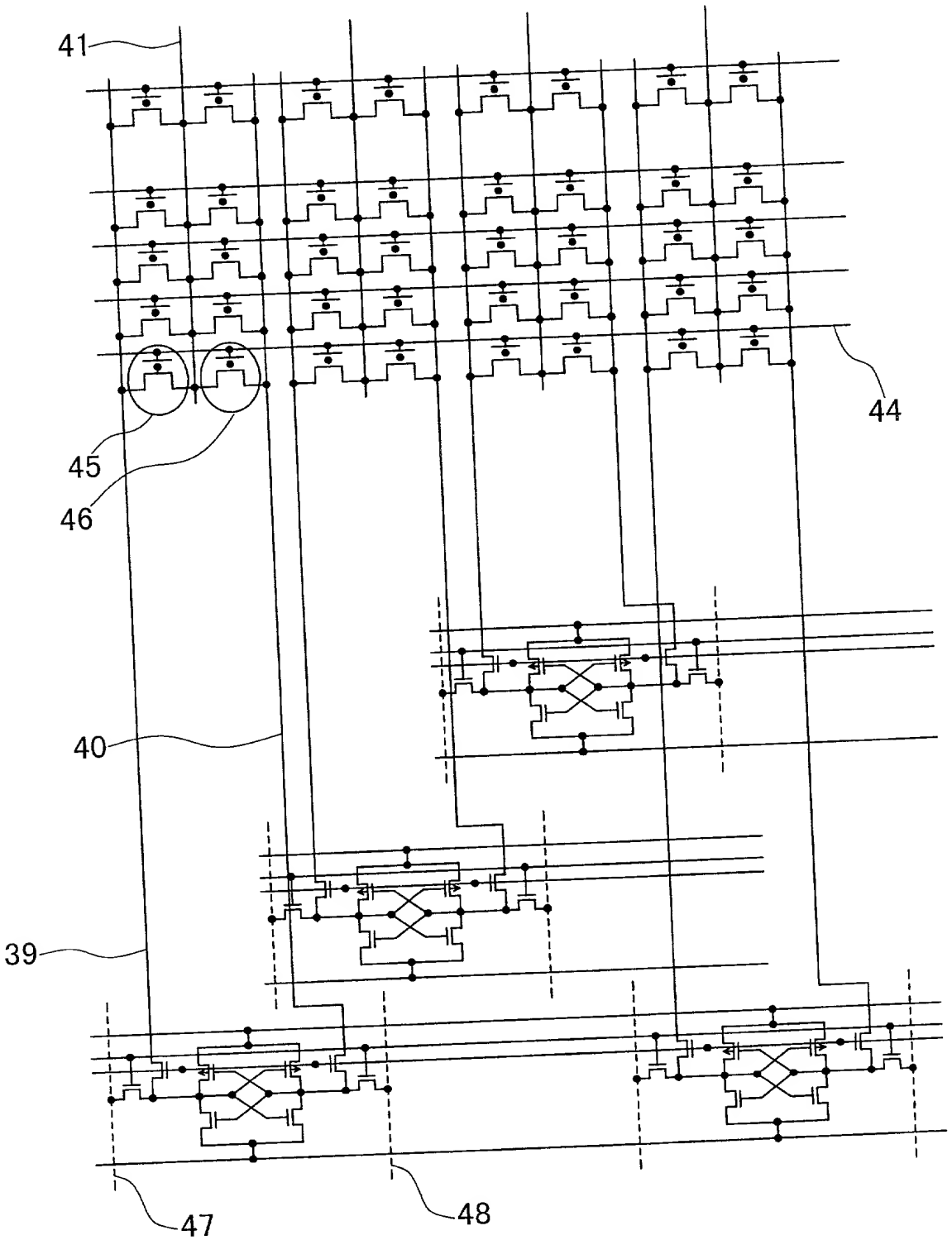


FIG.17

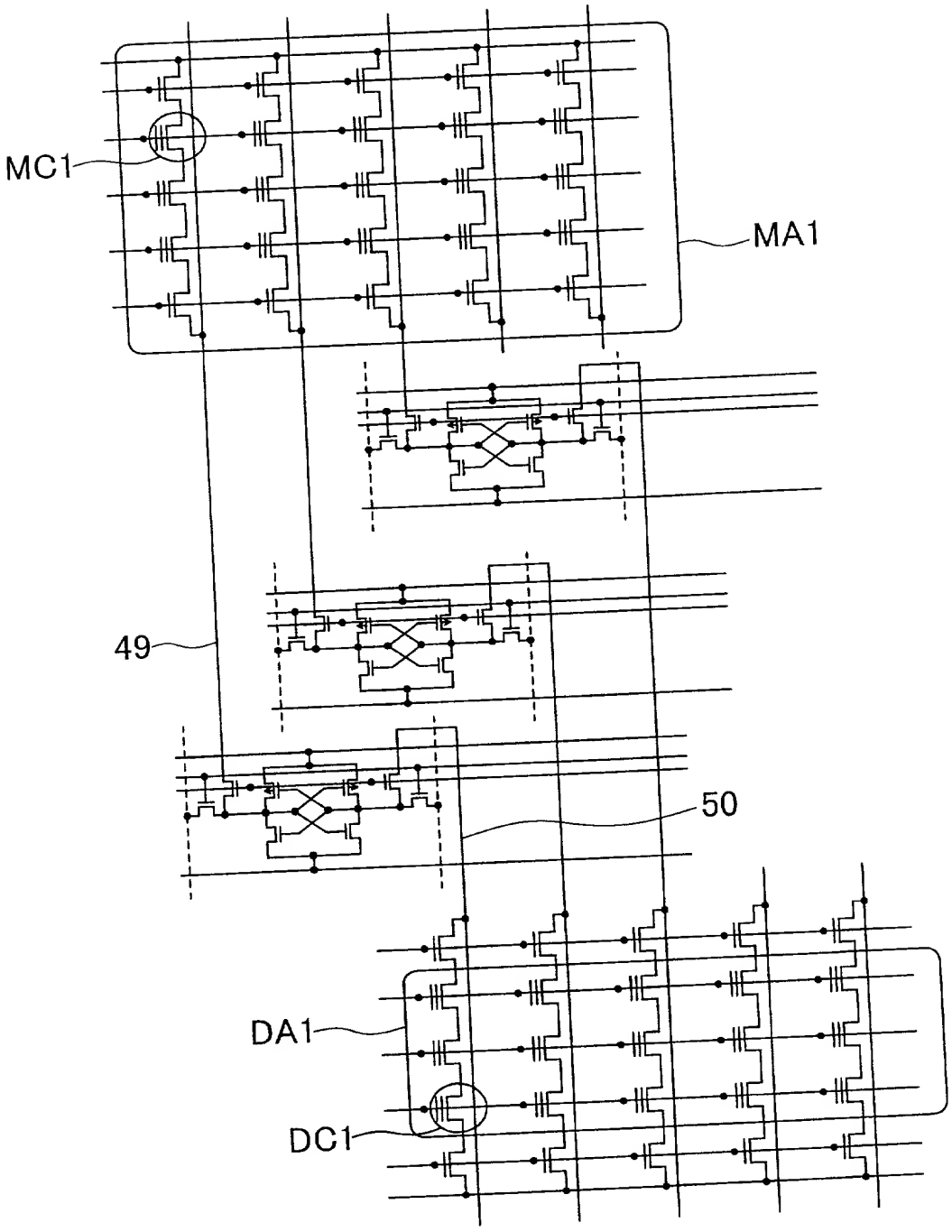


FIG.18a

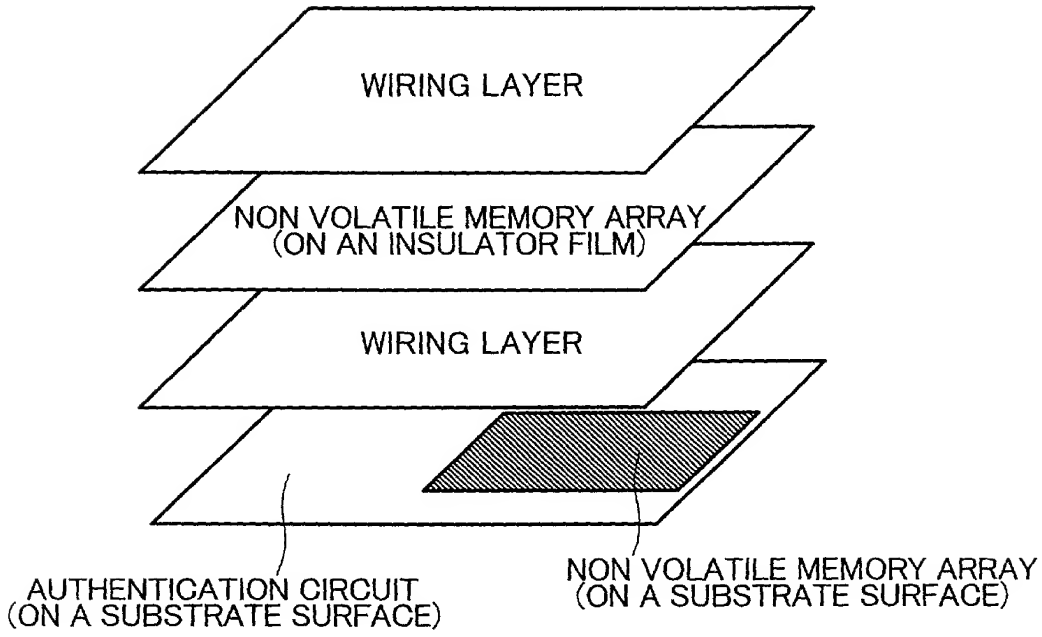


FIG.18b

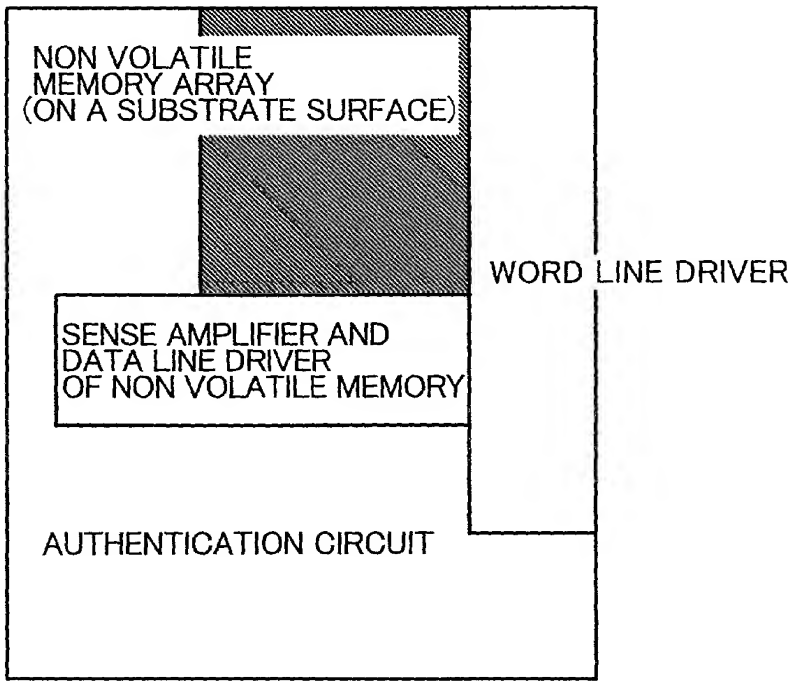


FIG.19a

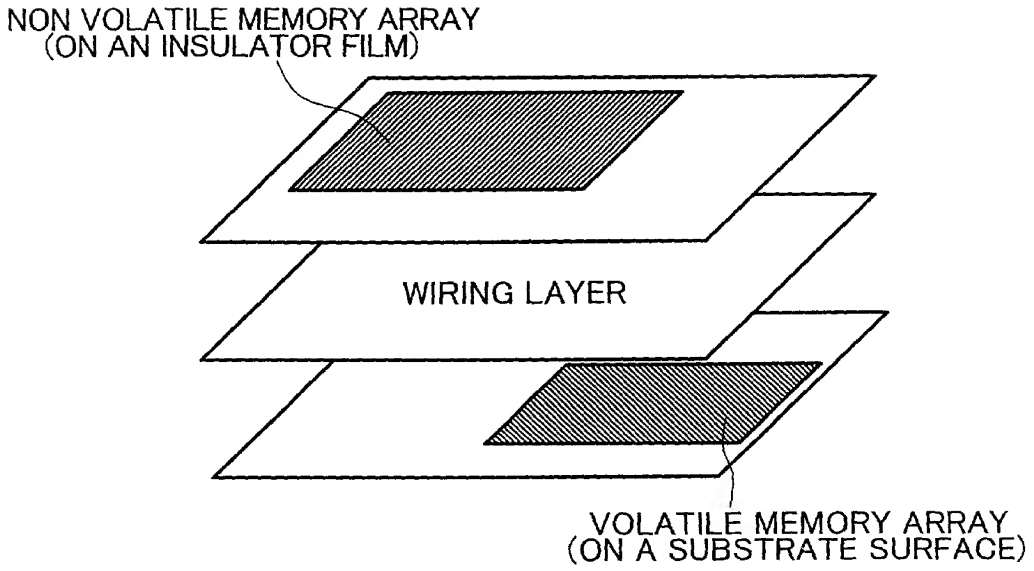


FIG.19b

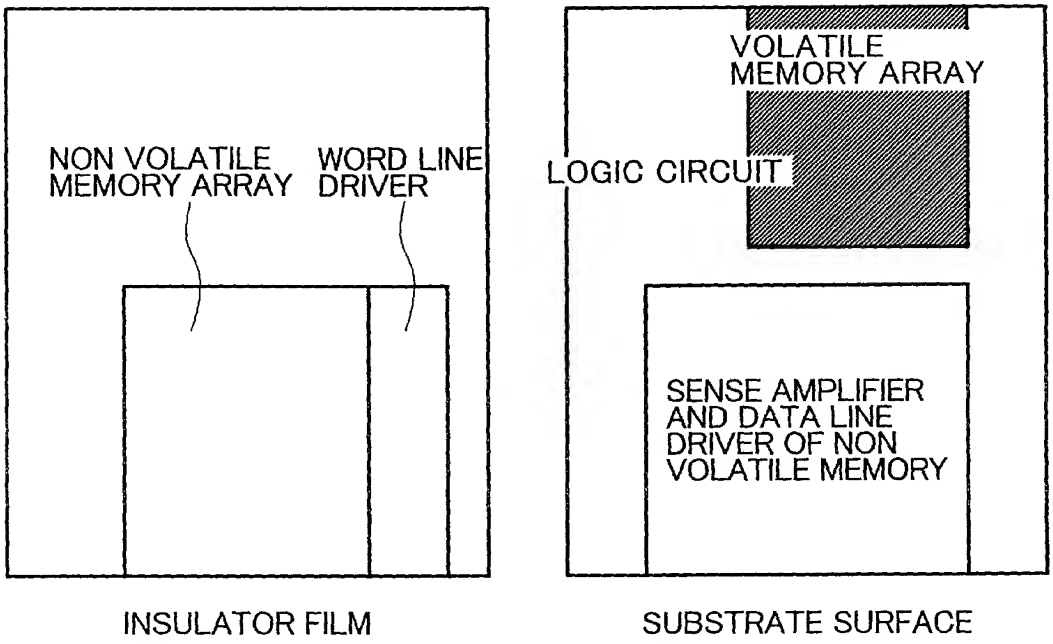


FIG.20

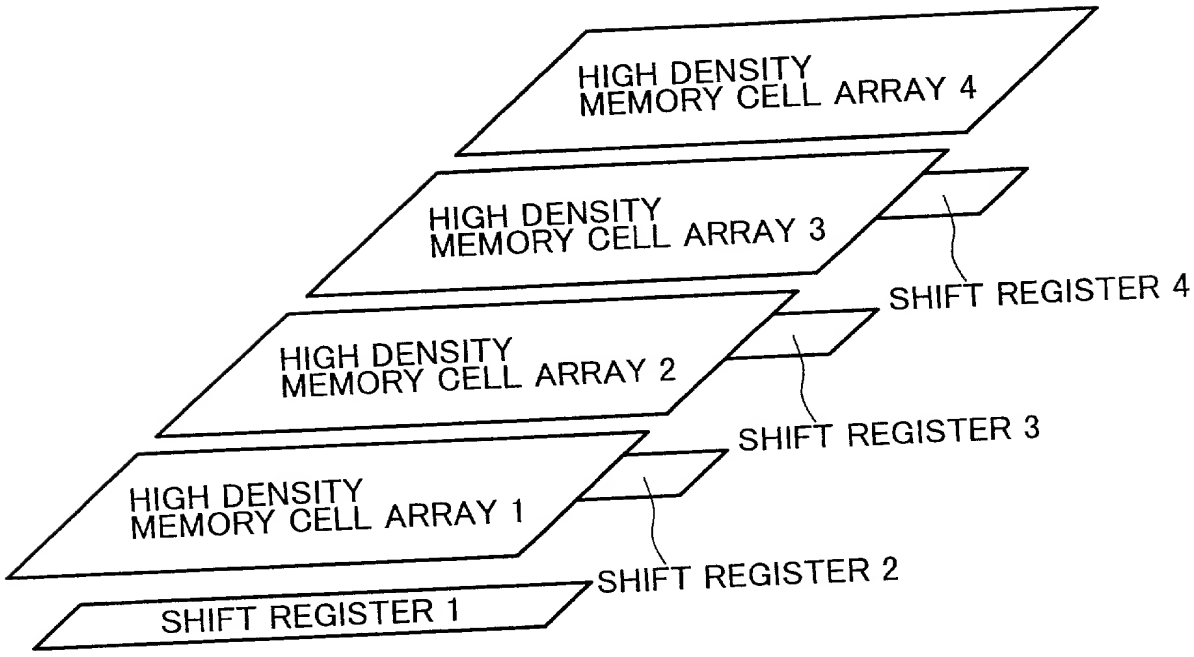

HIGH DENSITY
MEMORY CELL ARRAY 4
HIGH DENSITY
MEMORY CELL ARRAY 3
SHIFT REGISTER 4
HIGH DENSITY
MEMORY CELL ARRAY 2
SHIFT REGISTER 3
HIGH DENSITY
MEMORY CELL ARRAY 1
SHIFT REGISTER 2
SHIFT REGISTER 1

FIG.21

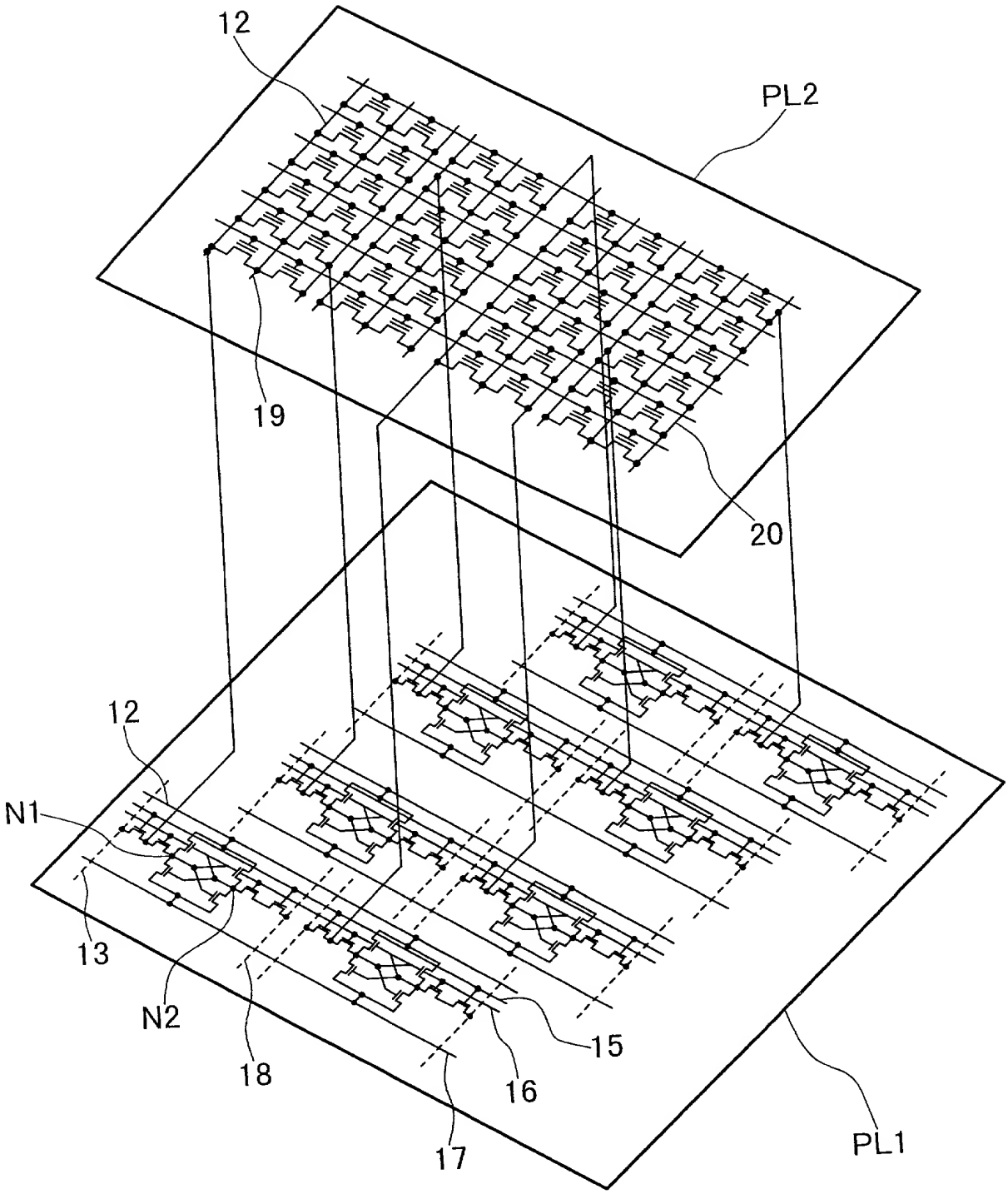
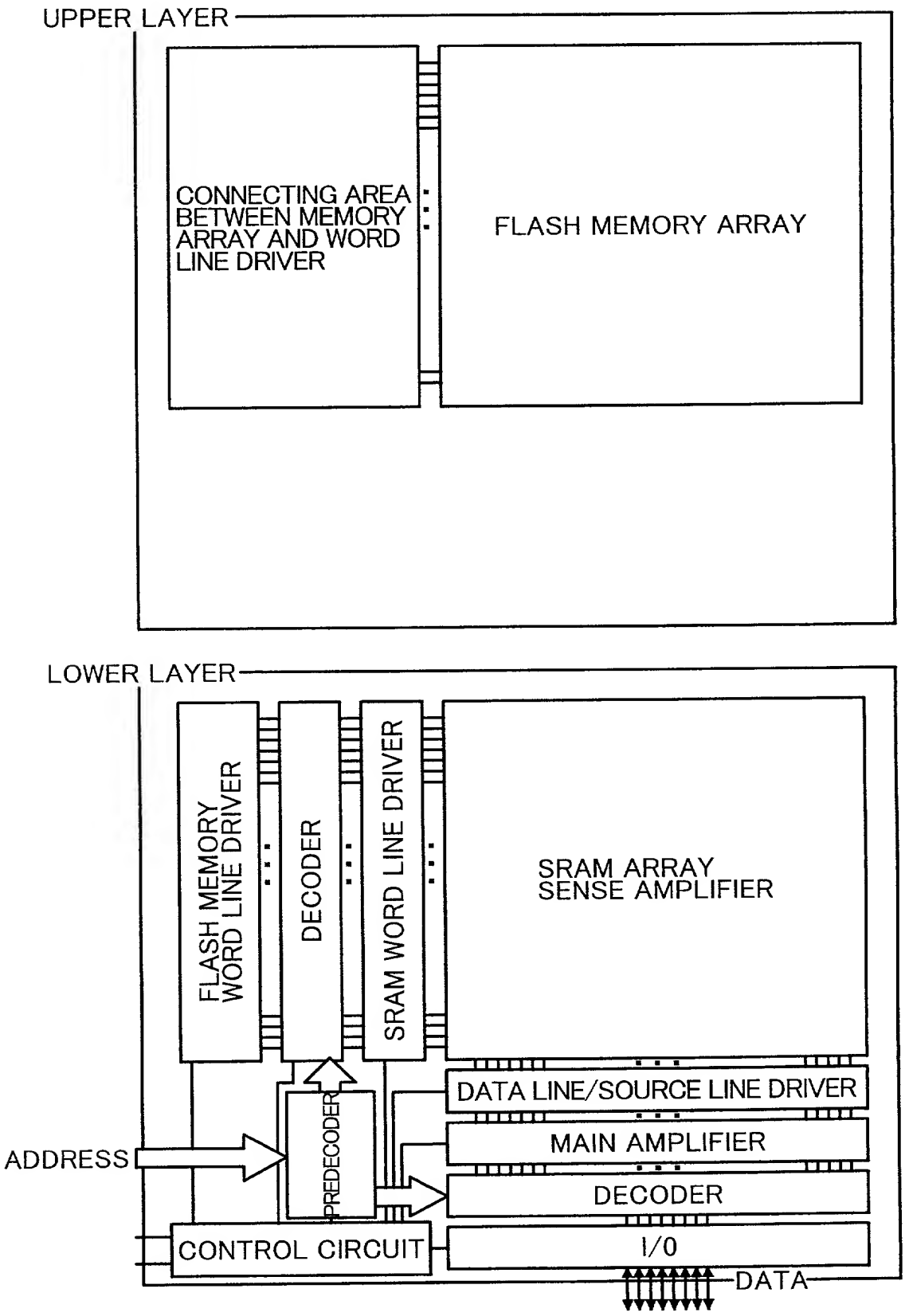


FIG.22


UPPER LAYER
CONNECTING AREA BETWEEN MEMORY ARRAY AND WORD LINE DRIVER
FLASH MEMORY ARRAY
LOWER LAYER
FLASH MEMORY WORD LINE DRIVER
DECODER
SRAM WORD LINE DRIVER
SRAM ARRAY SENSE AMPLIFIER
DATA LINE/SOURCE LINE DRIVER
MAIN AMPLIFIER
DECODER
I/O
DATA
ADDRESS
PREDECODER
CONTROL CIRCUIT